REMARKS

This Amendment seeks to place this application in condition for allowance. Several of the pending claims have been amended in order to more fully and/or definitely claim Applicants' invention, several of the pending claims have been found allowable, and new claims have been added in order to more fully protect Applicants' invention. Further, a Terminal Disclaimer is attached hereto to address the Examiner's concern of obviousness-type double patenting.

OFFICE ACTION

In the Office Action dated March 17, 1999, claim 151 was rejected under the judicially created doctrine of obviousness-type double patenting in light of claim 1 of U.S. Patent 5,481,540. Claims 152-156 and 164-167 were rejected under 35 U.S.C. § 112, 2nd paragraph. Claims 157-163 were allowed. Finally, claims 168-176 were rejected under 35 U.S.C. § 112, 1st and 2nd paragraphs. The rejections will be addressed in the order presented in the Action.

REJECTIONS -- 35 U.S.C. § 112, 1ST & 2ND PARAGRAPHS

Claims 168-176

Applicants have amended claim 168 to improve its clarity. This amendment also addresses the Examiner's concerns regarding 35 U.S.C. § 112, 1st and 2nd paragraphs. It should be noted, however,

that Applicants, to the extent understood, do not agree with the Examiner's interpretation of claim 168 (i.e., "a functional statement of intended result").

Further, it is Applicants' position that 35 U.S.C. § 112, sixth paragraph is not applicable to claim 168 and/or claims 169-176. In this regard, original claim 168 did not recite a step for performing a specified function. As such, 35 U.S.C. § 112, sixth paragraph does not appear to be pertinent. This notwithstanding, Applicants' amendment of claim 168 renders this issue moot.

Claims 152-156 and 164-167

Claims 152-154 and 165-166

Applicants have amended claims 152-154 and 165-166 to correct inadvertent typographical and grammatical errors and to more definitely and fully set forth the novel features of Applicant's invention. By doing so, Applicants believe they have also addressed the Examiner's concerns regarding these claims. No new matter has been added.

In particular, Applicants amendment to **claim 152** renders the rejection moot. This claim is believed to be fully supported by the specification as originally filed -- see, for example Figures 2 and 10; page 20, line 20 to page 21, line 20; and page 53, line 23 to page 59, line 2.

Applicants have amended **claim 153** to recite that "the value is representative of a number of clock cycles of the external clock." Applicants have amended **claim 165** to recite that the "value is representative of a fraction or whole number of clock cycles of the external clock." These claims are believed to be fully supported by the specification as originally filed -- see, for example page 39, lines 5-11. For the convenience of the Examiner, that text is reproduced immediately below:

> The value stored in a slave access-time register is preferably one-half the number of bus cycles for which the slave device should wait before using the bus in response to a request. Thus an access time value of '1' would indicate that the slave should not access the bus until at least two cycles after the last byte of the request packet has been received.

('200 Application, page 39, lines 5-11.

Applicants have amended **claim 154** and **claim 166** to recite "during an initialization sequence, the register stores the value." Support for this amendment is found at page 14, lines 13-21. In this regard, the specification states:

> Most of these registers can be modified and preferably are set as part of an initialization sequence that occurs when the system is powered up or reset. During the initialization sequence each device on the bus is assigned a unique device ID number, which is stored in the device ID register. A bus master can then use these

> device ID numbers to access and set appropriate registers in other devices, including access-time registers, control registers ....
> (the '200 Application, page 14, lines 13 to 22)

It is respectfully submitted that Applicants do not seek to claim how the value is stored in the register during the initialization sequence. Rather, Applicants' claim 154 and claim 166 describe when the value is stored in the register -- that is, during an initialization sequence.

Claim 164

Claim 164 has been amended to recite that the value stored in the programmable register "is representative of a number of clock cycles of an external clock to transpire before data is output onto an external bus in response to a read request." Accordingly, the output drivers, in response to the read request, output data onto the external bus "after the number of clock cycles of the external clock transpire." Support for such language is found at, for example, page 39, lines 5-11:

> The value stored in a slave access-time register is preferably one-half the number of bus cycles for which the slave device should wait before using the bus in response to a request. Thus an access time value of '1' would indicate that the slave should not access the bus until at least two cycles after the last byte of the request packet has been received.

In addition, support may be found in Figure 10 and page 53, line 23 to page 59, line 2.

Claims 155, 156 and 167

Claims 155, 156 and 167 were rejected because "it is not clear what the set register request is, and how the delay time is stored in the programmable register in response to the set register request." (Office Action of March 17, 1999, page 3). The operation of the set register request is set forth, for example, on: (1) page 14, line 13 to page 15, line 2; (2) page 23, line 12 to page 24, line 2; and (3) page 35, lines 19 to page 36, line 12. In this regard, the specification states:

> Most of these registers can be modified and preferably are set as part of an initialization sequence that occurs when the system is powered up or reset. During the initialization sequence each device on the bus is assigned a unique device ID number, which is stored in the device ID register. A bus master can then use these device ID numbers to access and set appropriate registers in other devices, including access-time registers, control registers, and memory registers, to configure the system.

(the '200 Application, page 14, lines 13 to 21)

...

> One special type of access is control register access, which involves addressing a selected register in a selected slave. In the preferred implementation of this

invention, AccessType[1:3] equal to zero indicates a control register request and the address field of the packet indicates the desired control register. For example, the most significant two bytes can be the device ID number (specifying which slave is being addressed) and the least significant three bytes can specify a register address and may also represent or include data to be loaded into that control register. Control register accesses are used to initialize the access-time registers .... Control register access can also be used to initialize or modify other registers ....

(the '200 Application, page 23, line 12 to page 24, line 2)

...

In the bus-based system of this invention, a mechanism is provided to give each device on the bus a unique device identifier (device ID) after power-up or under other conditions as desired or needed by the system. A master can then use this device ID to access a specific device, particularly to set or modify registers of the specified device, including the control and address registers. In the preferred embodiment, one master is assigned to carry out the entire system configuration process. The master provides a series of unique device ID numbers for each unique device connected to the bus system. ... The configuration master should check each device, determine the device type and set appropriate control registers, including access-time registers.

(the '200 Application, page 35, line 20 to page 36, line 12)

It should be noted that preferred embodiments/techniques to reset or initialize the device identification code for the integrated circuit device is set forth in considerable detail between page 36, line 13 to page 39, line 21.

NONSTATUTORY DOUBLE PATENTING

To address the concern regarding double patenting in light of the parent patent, namely U.S. Patent 5,841,540, Applicants submit herewith a Terminal Disclaimer executed by the attorney of record in this application. Applicants believe that this Terminal Disclaimer complies fully with the relevant parts of 37 C.F.R. § 1.321.

ALLOWED CLAIMS

Claims 157-163 were allowed. (See, Office Action of March 17, 1999, page 1).

NEWLY SUBMITTED CLAIMS

The new claims submitted in this Amendment have been added to more definitely and fully protect Applicants' invention. No new matter has been added.

For many of the same reasons discussed above relative to the originally filed claims, the newly submitted claims are believed to

be fully supported by the specification as originally filed. In this regard, see, for example:

Figures 2 and 10; and
page 14, line 3 to page 15, line 2;
page 15, lines 18-22;
page 20, line 20 to page 21, line 20;
page 23, line 12 to page 24, line 2;
page 39, lines 5-11;
page 46, line 19 to page 48, line 17; and
page 53, line 23 to page 59, line 2.

AMENDMENT TO SPECIFICATION

Applicants have amended the specification to correct obvious spelling, typographical and grammatical errors. Moreover, the specification has been amended to correspond to new Figure 16 -- as is discussed immediately below. No new matter has been added.

AMENDMENT TO THE DRAWINGS

New Figure 16, attached hereto, is added to illustrate, among other things, access-time register(s) 173. Figure 16 illustrates one embodiment of the internal registers within each device illustrated in Figure 2. Support may be found in the specification at page 14, lines 3-21 and page 53 lines 4-21. No new matter has been added.

Moreover, the specification has been amended to correspond to new Figure 16. No new matter has been added.

By way of note, the amendment to the drawings and the corresponding amendment of the specification is similar to the amendment made in the application leading to U.S. Patent 5,841,580. As noted above, the '580 patent is the parent of this application.

CONCLUSION

Applicants request entry of the foregoing amendment prior to examination of this application. Applicants submit that all of the claims present patentable subject matter which definitely set forth the novel and unobvious features of Applicants' invention. Accordingly, Applicants respectfully request allowance of all of the claims.

It is noted that should a telephone interview expedite the prosecution in any way, the Examiner is invited to contact Neil Steinberg at 703-264-3521.

Respectfully submitted,

Date: March 23, 1999

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